REV-01
MCA/46/51

2023/12

SET A

MASTER OF COMPUTER APPLICATION
FIRST SEMESTER
COMPUTER ORGANIZATION & ARCHITECTURE
MCA-101

[USE OMR SHEET FOR OBJECTIVE PART]

Duration: 3 hrs. Full Marks: 70

Objective

Time: 30 mins. Marks: 20

Choose the correct answer from the following: ***1×20=20***

1. A computer program that converts entire program into machine language at a time is:
   a. Assembler b. Compiler
   c. Interpreter d. None
2. How many select lines would be required for an 16 : 1 MUX?
   a. 2 b. 4
   c. 8 d. 3
3. How many AND gates are required to construct a 4:1 MUX?
   a. 2 b. 3
   c. 5 d. 4
4. Which of the following is responsible for arithmetic and logic operations?
   a. ALU b. Memory
   c. Control Unit d. All the above
5. CPU consists of:
   a. ALU & Memory b. ALU & Control Unit
   c. Control Unit & Memory d. All the above
6. Booth multiplication algorithm looks after multiplication with negative number as.....
   a. 2's Complement b. 1's complement
   c. Signed Magnitude d. None
7. Which of the following is called data distributor?
   a. MUX b. DEMUX
   c. Encoder d. Decoder
8. In 8-bit microprocessor, how many opcodes are possible?
   a. 246 b. 278
   c. 250 d. 256
9. Which of the following is unidirectional?
   a. Address bus b. Data bus
   c. Both a & b d. None
10. Which of the following is a special purpose register of microprocessor?
    a. Program counter b. Instruction register
    c. Accumulator d. None

11. During a write operation if the required block is not present in the cache then..... occurs.
    a. Write miss
    b. Write latency
    c. Write hit
    d. Write delay

12. The bit used to indicate whether the block was recently used or not is.....
    a. Reference bit
    b. Dirty bit
    c. Control bit
    d. Idol bit

13. Any condition that causes a processor to stall is called as.....
    a. Hazard
    b. Page fault
    c. System error
    d. None of the mentioned

14. The computer cluster architecture emerged as a result of.....
    a. ISA
    b. Workstation
    c. Super computers
    d. Distributed systems

15. In the client server model of the cluster..... approach is used.
    a. Load configuration
    b. FIFO
    c. Bankers algorithm
    d. Round robin

16. The CISC stands for.....
    a. Computer Instruction Set Compliment
    b. Complete Instruction Set Compliment
    c. Computer Indexed Set Components
    d. Complex Instruction set computer

17. The iconic feature of the RISC machine among the following is.....
    a. Reduced number of addressing modes
    b. Increased memory size
    c. Having a branch delay slot
    d. All of the mentioned

18. Pipe-lining is a unique feature of.....
    a. RISC
    b. CISC
    c. ISA
    d. IANA

19. The pipelining process is also called as.....
    a. Superscalar operation
    b. Assembly line operation
    c. Von Neumann cycle
    d. None of the mentioned

20. In binary multiplication, the multiplier is stored in.....
    a. PC Register
    b. Shift register
    c. Cache
    d. None of the mentioned

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Descriptive

Time : 2 hr. 30 mins. Marks : 50

[Answer question no.1 & any four (4) from the rest]

1. Explain the following instruction with RTL. 10
   i) LDA ii) BUN iii) STA iv) ADD v) CIR
2. a) Explain with a suitable block diagram of the Control Unit of Basic Computer. 5+5=10
   b) State & Prove De' Morgan's theorems.
3. a) Realize a full adder circuit using two half adders circuits. 5+5=10
   b) What is Universal gate? Realize an OR gate using NAND gates only.
4. a) What do you mean by Addressing modes? Discuss various addressing modes of 8085 microprocessor. 5+5=10
   b) Describe general register organization of a basic computer. Define control word.
5. a) Write an Assembly program to add two numbers. 5+5=10
   b) Explain the organization of Status register of a basic computer with neat diagram.
6. What is the role of peripheral devices? How DMA is used to control memory transfer without CPU's intervention? Explain. 4+6=10
7. a) What is pipeline processing? Explain with a suitable example. 5+5=10
   b) What is Interrupt? Define Priority interrupt. Write a short note on UART.
8. Explain Booth's multiplication algorithms with a suitable example. 10

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