2017/12

M.Sc. ELECTRONICS
THIRD SEMESTER
COMPUTER ORGANIZATION (MDC)
MCA-507

Duration: 3 Hrs. **Marks: 70**

PART : A (OBJECTIVE) = 20
PART : B (DESCRIPTIVE) = 50

[PART-B : Descriptive]

Duration: 2 Hrs. 40 Mins. **Marks: 50**

[Answer question no. One (1) & any four (4) from the rest]

1. What is Memory Hierarchy in computer system? Explain it in details. (10)
2. Explain DMA with suitable diagram. (10)
3. Define RISC & CISC. What is Stack Organization? Explain with a suitable example. (4+6=10)
4. Convert the given into Polish & Reverse Polish Notation: (5+5=10)
   (A+B)*(C*(D+E)+F)
5. What do you understand by Instruction format? Write the following equation in 3 address instruction & 1 address instruction mode. (5+5=10)
   X=(A+B) * (C+D)
6. Define addressing modes and its types in detail. (10)
7. What is Interrupt? Differentiate between Vectored & Non-Vectored interrupt. (4+6=10)
8. Write short notes on: (5+5=10)
   a) Data Transfer Instruction.
   b) Program Control Instruction.

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[PART-A : Objective]

Choose the correct answer from the following: **1×20=20**

1. FPGA means:
   a. Field Programmable Gate Array.
   b. Forward Programmable Gate Array.
   c. Forward Parallel Gate Array.
   d. Field Parallel Gate Array.

2. What is meant by ALU?
   a. Arithmetic logic upgrade.
   b. Arithmetic logic unit.
   c. Arithmetic logic unsigned.
   d. Arithmetic local unsigned.

3. Which one of the following is not a vectored interrupt?
   a. TRAP.
   b. INTR
   c. RST 3.
   d. RST 7.5.

4. HLT opcode means:
   a. load data to accumulator.
   b. store result in memory.
   c. load accumulator with contents of register.
   d. end of program.

5. Type of ROM which is manufactured without having any initial storage in it is termed as:
   a. PROM
   b. EROM
   c. BROM
   d. DROM

6. Access store from which data can be read and can be written on it is classified as:
   a. read only memory.
   b. random access memory.
   c. random only memory.
   d. read access memory.

7. Switching from one process to another. This swapping is called a:
   a. Process switch.
   b. Context switch.
   c. Exchange.
   d. Both a and b.

8. Flash memories have limited number of block's write cycles, these cycles must be at least:
   a. 1000
   b. 10,000
   c. 100,000
   d. 100,000,00

9. In 32-bit addressing mode, address field is either 1 byte or:
   a. 2 bytes
   b. 3 bytes
   c. 4 bytes
   d. 5 bytes

10. If a comparing instruction and branch instruction uses some architectures, to treat these comparisons chooses as:
    a. Error
    b. Exceptions
    c. Special cases
    d. All above

11. Addressing mode which is set to index arrays, is applied to indexed addressing mode, in computers is:
    a. Scaled addressing mode.
    b. Register indirect addressing mode.
    c. Register addressing mode.
    d. Immediate addressing mode.

12. Simplest scheme to handle branches is to:
    a. Flush pipeline.
    b. Freezing pipeline.
    c. Depth of pipeline.
    d. Both a and b.

13. The DMA transfers are performed by a control circuit called as:
    a. Device interface
    b. DMA controller
    c. Data controller
    d. Overlooker

14. DMA stands for:
    a. Direct Memory Access
    b. Double Memory Access
    c. Duplicate Memory Access
    d. None of the above

15. Which is not a type of Interrupt?
    a. Vectored
    b. Non-Vectored
    c. Priority
    d. Accessible

16. After the completion of the DMA transfer the processor is notified by:
    a. Acknowledge signal.
    b. Interrupt signal.
    c. WMFC signal.
    d. None of the above.

17. The DMA controller has_____ registers.
    a. 1
    b. 2
    c. 3
    d. 4

18. The controller is connected to the_____.
    a. Processor BUS.
    b. System BUS.
    c. External BUS
    d. None of the above.

19. The technique where the controller is given complete access to main memory is:
    a. Cycle stealing.
    b. Memory stealing.
    c. Memory Con.
    d. Burst mode.

20. The registers of the controller are_____.
    a. 64 bits
    b. 34 bits
    c. 32 bits
    d. 16 bits

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UNIVERSITY OF SCIENCE & TECHNOLOGY, MEGHALAYA

[PART (A) : OBJECTIVE]

Duration : 20 Minutes

Serial no. of the main Answer sheet

Course : .....

Semester : ..... **Roll No :** .....

Enrollment No : ..... **Course code :** .....

Course Title : .....

Session : 2017-18 **Date :** .....

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Instructions / Guidelines

- The paper contains twenty (20) / ten (10) questions.
- Students shall tick (✓) the correct answer.
- No marks shall be given for overwrite / erasing.
- Students have to submit the Objective Part (Part-A) to the invigilator just after completion of the allotted time from the starting of examination.

Full Marks	Marks Obtained
20	

Scrutinizer's Signature *Examiner's Signature* *Invigilator's Signature*