MASTER OF COMPUTER APPLICATION
First Semester
DIGITAL SYSTEM
(MCA - 102)

Duration: 3Hrs. **Full Marks: 70**

Part-A (Objective) =20
Part-B (Descriptive) =50

(PART-B: Descriptive)

Duration: 2 hrs. 40 mins. **Marks: 50**

Answer any *four* from *Question no.* 2 to 8
***Question no.* 1 is compulsory.**

1. (a) Convert the following numbers to binary. (2×3=6)

   a. $254_{(10)}$

   b. $56_{(8)}$

   c. $1A4_{(16)}$

   (b) Define ASCII and EBCDIC Code. (4)

2. (a) Why NAND and NOR gate is known as universal gates? (6)

   (b) Explain canonical logic forms with examples. (4)

3. Given the Boolean Function: (3+3+4=10)

   $F = x'yz + xz$

   a. Draw the logic diagram of the original expression.

   b. Simplify the function using Boolean algebra.

   c. Obtain the truth table.

4. (a) Describe Full Subtractor with truth table and logic diagram. (7)

   (b) Construct the Full Adder using two Half Adders and OR gates. (3)

5. (a) Discuss the main features of SR Flip Flop and Positive Edge Triggered SR Flip Flop. (3+3=6)

   (b) Explain the operations of Master-Slave JK Flip Flop. (4)

6. (a) Describe the functional block diagram of a CPU. (5)

(b) What are the semi-conductor memories available in memory devices? Explain. (5)

7. (a) Design a Mod-6 negative edge triggered up counter. (4)

(b) For a 3-bit shift register, explain the operation for the following categories with the help of block diagram. (6)

a. Serial in – serial out

b. Serial in – parallel out

c. Parallel in – parallel out

8. Simplify the following using K-map. (4+6=10)

a. $F = \sum (2,3,4,5,6,7,9,12,13,14,15)$

b. $F = ab + ab'c + a'bc' + bc'$

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Duration: 20 minutes **Marks – 20**

(PART A - Objective Type)

I. Choose the correct answer: **1×20=20**

1. The minterm in K-map are marked with a
   a. y b. x c. 0 d.1
2. x+xy =?
   a. y b. x c. xy d. None
3. (a+b+c)'=
   a. a'b'c' b. a'+b'+c' c. abc d. a+b+c
4. Full Adder performs addition of _____ bits.
   a. 2 b. 3 c. 4 d. 5
5. 8 to 1 multiplexer would have:
   a. 1 output b. 2 output c. 3 output d. None
6. 1's complement of 11001010 is
   a. 01010101 b. 00110101
   c. 00001010 d. None of the above
7. One that is not the type of flip flop is:
   a. JK b. T c. RS d. ST
8. A binary variable takes the values:
   a. 0 only b. 0 and 1
   c. 0 and -1 d. 1 and 2
9. One that is not a gate:
   a. NOT b. AND c. OR d. XNOT
10. Which number system has a base 16?
    a. Decimal b. Octal
    c. Hexadecimal d. None
11. In an SR Flip Flop built from NAND gate, which condition is not allowed?
    a. S=0, R=0 b. S=0, R=1
    c. S=1, R=0 d. S=1, R=1

12. Which of these sets of logic gates are designated as universal gates?
    a. NOR, NAND
    b. XOR, NOR, NAND
    b. OR, NOT, AND
    d. NOR, NAND, XNOR

13. In the toggle mode a JK Flip Flop has
    a. J=0, K=0
    b. J=1, K=1
    c. J=0, K=1
    d. J=1, K=0

14. If a hexadecimal number needs to convert to binary, for how many hexadecimal digits, there will be how many bits?
    a. 1 b. 2 c. 4 d. 8

15. In Boolean Algebra, A.A is equal to
    a. A b. A^2 c. 2A d. 1

16. Complement of NOR and OR gate is _____ and _____ respectively.
    a. AND, NAND
    b. NAND, AND
    c. OR, NOR
    d. NOR, OR

17. EBCDIC is the full form of _____.
    a. Extended Bit Coded Decimal Interchange Code
    b. Extended Binary Coded Detection Interchange Code
    c. Extended Binary Color Decimal Interchange Code
    d. Extended Binary Coded Decimal Interchange Code

18. How many inputs and outputs are required for demultiplexer?
    a. One input and one output.
    b. Number of selection inputs and one output.
    c. One input and many outputs.
    d. None of the above.

19. What is the requirement of Full Subtractor Circuit?
    a. 3 inputs and 2 outputs.
    b. 3 inputs and 1 output.
    c. 2 inputs and 2 outputs
    d. 2 inputs and 3 outputs.

20. Master Slave Flip Flop consists of _____ Flip Flop(s)
    a. 1 b. 2 c. 3 d. 4

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