REV-01
BCA/03/08

2023/06

SET A

BACHELOR OF COMPUTER APPLICATION
SECOND SEMESTER
COMPUTER ORGANIZATION
BCA-921 (1DMn)

[USE OMR SHEET FOR OBJECTIVE PART]

Duration: 1hr. 30 mins. **Full Marks: 35**

Objective

Time: 15 mins. **Marks: 10**

Choose the correct answer from the following: ***1×10=10***

1. The operation of performing the logical AND, OR, and NOT operations on bits is known as:
   a. Multiplexing
   b. Demultiplexing
   c. Encoding
   d. Boolean algebra

2. The arithmetic logic unit (ALU) of a computer performs which of the following operations?
   a. Addition and subtraction only
   b. Multiplication and division only
   c. Logical operations and data manipulation
   d. All of the above

3. The concept of pipelining in computer architecture is primarily used to:
   a. Increase the clock speed of the CPU
   b. Increase the size of the cache memory
   c. Improve the efficiency of instruction execution
   d. Reduce the number of registers in the CPU

4. Which of the following memory types provides the fastest access time?
   a. Cache memory
   b. Main memory (RAM)
   c. Secondary storage (Hard disk)
   d. Virtual memory

5. Which of the following is an example of a volatile memory?
   a. Hard disk
   b. Flash memory
   c. RAM
   d. DVD-ROM

6. The control unit of a CPU communicates with other system components through:
   a. Buses
   b. Registers
   c. ALU
   d. Cache memory

7. The process of converting a binary number into its decimal equivalent is known as:
   a. Encoding
   b. Decoding
   c. Conversion
   d. Translation

8. A half adder is a combinational logic circuit that performs:
   a. Addition of two binary numbers with carry-in and carry-out
   b. Subtraction of two binary numbers with borrow-in and borrow-out
   c. Multiplication of two binary numbers
   d. Division of two binary numbers

9. The inputs of a half adder are:
   a. Two binary numbers and a carry-in
   b. Two binary numbers only
   c. A binary number and a carry-in
   d. A binary number and a carry-out

10. Which gate(s) are used in the implementation of a half adder?
   a. XOR gate only
   b. AND gate only
   c. OR gate only
   d. XOR gate and AND gate

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Descriptive

Time : 1 hr. 15 mins. **Marks : 25**

[Answer question no.1 & any two (2) from the rest]

1. Explain the evaluation of computer technology from the first generation to the fifth generation. 5

2. Explain with a suitable block diagram of the functional units of the Computer. Also briefly describe the primary and secondary computer storage's operations. 5+5=10

3. A computer has a cache, main memory, and a disk used for virtual memory. Access to the cache takes 10 ns. Access to main memory takes 100 ns. Access to the disk takes 10,000 ns. Suppose the cache hit ratio is 0.9 and the main memory hit ratio is 0.8. Calculate the effective access time required to access a referenced word on the system. 10
   a) Simultaneous access memory organization is used.
   b) Hierarchical access memory organization is used.

4. Answer the following questions: 5
   a) What is a System Bus? Why do you need Bus? Write and explain the components used by the System bus.
   b) What do you mean by Pipelining in Computer Architecture? What are the major characteristics of a Pipeline? Explain briefly the different stages of pipelining. 5

5. Answer *any one* of the following questions:
   a) Realize a full adder circuit using two half adder circuits. . 5
   b) Given **A**= 10110 **B**= 10010, then compute **A** X **B** with the suitable algorithm. 5

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