BCA

SECOND SEMESTER (SPECIAL REPEAT) COMPUTER ORGANIZATION & ARCHITECTURE

		1-202				
(Use separate answer scripts for Objective & Des Duration: 3 hrs.			Full Marks: 70			
		Objective)				
Tim	Time: 20 min. (PART-A: Objective) Marks: 20					
Choose the correct answer from the follow		owing:	1×20=20			
1.	What is the decimal equivalent of (3F) ₁₆ ?					
	a. 63	b. 32				
	c. 16	d. 38				
2.	Hit ratio is a term used to measure of cache memory.					
	a. Size	b. Speed				
	c. Performance	d. Data transfer rate				
3.	Bootstrap loader program is stored in	memory.				
	a. Virtual	b. RAM				
	c. Cache	d. ROM				
4.	De Morgan's second theorem says that N	a bubbled gate.				
	a. AND	b. XAND				
	c. XOR	d. OR				
5. In one-address instruction, second address is implied to a processor register of						
	a. Accumulator	b. MAR	8			
	c. Instruction Register	d. Program Counter				
6.	PUSH and POP are example of	address instruction				
0.	a. Zero	b. One				
	c. Two	d. Three				
7.	A data transfer technique used by DMA such that the controller transfer one data word					
	at time is called	b. Serial transfer				
	a. Cycle stealing c. Burst transfer	d. Sequence transfer				
8.	Which one of the following is NOT a vali		or?			
	a. Supervisor	b. Overflow				
	c. Equal	d. NAN				
9.	The register contains the address of an instruction to be fetched is called					
	a. Instruction register	b. Program counter				
	c. Memory Address Register (MAR)	d. Memory Buffer Reg	ister (MBR)			
10.	The simplified form of the Boolean expression $(X + Y + XY)(X + Z)$ is					
	a. $X + Y + Z$	b. XY + YZ				
	c X + Y7	d. XZ + Y				

11.	The number of Segment register consist in a. Three	b. Five		
	c. Six	d. Eight		
12.	How many memory locations can 14 addre			
	a. 16,384	b. 8,192		
	c. 4096	d. 14		
13.	3. Conversion of an octal number 7432 ₈ to a binary number is			
	a. 1111000110111 ₂	b. 111100011010 ₂		
	c. 110011010111 ₂	d. 1111111111000 ₂		
14.	In PowerPC processor, there are 32 genera	I purpose register each of size		
	a. 8 bits	b. 16 bits		
	c. 32 bits	d. 64 bits		
15.	Call/Return behavior of PowerPC is deter	mined by a register called		
	a. Condition Register	b. Count register		
	c. Link register	d. Exception register		
16				
10.	Which of the following is NOT match prop			
	Processor Year of Developm 1. IBM 1973	lent		
	2. VAX 1978			
	3. SPARC 1987			
	4. PowerPC 1990			
	a. 1	b. 2		
	c. 3	d. 4		
17.	7. The number of general purpose register in MIPS R10000 processor is			
	a. 8	b. 16		
	c. 32	d. 64		
10				
18.	Two assessment factors are used to mitiga	te the controversy between RISC vs. C		
	They are &	F G 18 B G		
	a. Register number & Memory capacityc. Quantitative & Qualitative			
		d. Perfective & Quantitative		
19.	SPARC processor was developed by			
	a. Motorola	b. Intel Co.		
	c. IBM Co.	d. Sun Microsystems		
20.	0. The design issue of Superscalar processor utilize of			
	a. RISC	b. Instructions pipelines		
	c. More registers	d. SPARC		

(PART-B: Descriptive)

Ti	Marks: 50	
	[Answer question no.1 & any four (4) from the rest]	
1.	What do you mean by bus? What are the different types of busses that a processor has? Explain PCI bus.	2+1+7=10
2.	a. Explain the hardware architecture of Intel 8085 microprocessor.b. What are the controversy between CISC and RISC technology?	5+5=10
3.	Explain primary memory, secondary memory and cache memory. State what type of memory is used for each of these memories.	7+3=10
4.	What do you mean by control unit? Explains hardwired control unit with block diagram.	3+7=10
5.	a. What are the basic characteristics of CISC technology? b. Write an assembly program to add two numbers.	5+5=10
6.	What do you mean by computer instruction? Explain the basic computer instruction format.	3+7=10
7.	a. Explain the function of DMA controller in memory transfer with block diagram.	5+5=10
	b. Explain the register organization of a Pentium processor with a block diagram.	
8.	a. Explain the functions of IOP. b. Discuss interrupt driven data transfer mode of computer.	5+5=10

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