BACHELOR OF COMPUTER APPLICATION
SECOND SEMESTER (REPEAT)
DIGITAL LOGIC AND DESIGN
BCA-201

Duration : 3 hrs.

Full Marks : 70

(**PART-A : Objective**)

Time : 20 min.

Marks : 20

Choose the correct answer from the following:　　　　　　*1X20=20*

1. In which of the following gates, the output is 1, if and only if at least one input is 1.
   a. AND
   b. OR
   c. NOT
   d. NAND

2. Adding of 1001 and 0010 gives output
   a. 1011
   b. 1111
   c. 0
   d. 1010

3. $x+x'y=$
   a. x
   b. Y
   c. x+y
   d. x-y

4. Which of the following gates are added to the input of OR gate to convert it to the NAND gate
   a. NOT
   b. OR
   c. AND
   d. XOR

5. Which of the following expression is not equivalent to 'X'
   a. X NAND X
   b. X NOR X
   c. X NAND 1
   d. X NOR 1

6. A 1-to 4 line de-multiplexer is to be implemented using a memory. How many bits must each word have?
   a. 1
   b. 2
   c. 4
   d. 8

7. The XNOR gate is equivalent to which gate followed by an inverter?
   a. OR
   b. AND
   c. NAND
   d. XOR

8. One that is not postulate of Boolean Algebra
   a. Commuitive
   b. Duality
   c. Assosiativity
   d. Identity element

9. Which table shows logical state of digital circuit for every
   a. Functional table
   b. Truth table
   c. Execution table
   d. ASCII table

10. In of D excitation table flip flop next state is equal to
   a. Present state   b. Next state
   c. Input state   d. D state

11. Product of 1011 and 101
   a. 110111   b. 110011
   c. 111011   d. 111100

12. The sum of two n-bit binary numbers can be done
   a. Serially   b. parallely
   c. Sequentially   d. Both a and b

13. A combinational circuit that selects one from many inputs
   a. Encoder   b. Decoder
   c. MUX   d. DEMUX

14. The minterms in a K-map are marked with a
   a. X   b. Y
   c. 0   d. 1

15. Full adder performs addition on
   a. 2 bits   b. 3 bits
   c. 4 bits   d. 5 bits

16. Digital number is said to be of base or radix
   a. 8   b. 10
   c. 2   d. 0

17. ASCII stands for
   a. African Standard Code for Information   b. American Standard Code for Integer
      Interchange   Interchange
   c. American Standard Code for   d. African Standard Code for Integer
      Information Interchange   Interchange

18. A binary variable can take the values
   a. 0 only   b. 0 and 1
   c. 1 and 2   d. None of these

19. $(a+b+c)' =$
   a. $a'b'c'$ b. $a'+b'+c'$
   c. $a\,b\,c$ d. $a+b+c$

20. Odd parity of word can be conveniently tested by
   a. OR gate   b. AND gate
   c. NOR gate   d. XOR gate

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[**PART-B : Descriptive**]

Time : 2 hrs. 40 min.   Marks : 50

[Answer question no.1 & any four (4) from the rest]

1. Describe AND, OR, NOT, NOR, NAND, XOR, XNOR gates with their   10
   truth tables and logic gates

2. Simplify using Boolean theorems   3+3+4=10

   i) $B=\overline{X}Y+XY+X\overline{Y}+\overline{X}\,\overline{Y}$
   ii) $Z=AB\overline{C}+A\overline{B}C+A\overline{B}C+A\overline{B}\,\overline{C}$
   iii) $Y=XY+\overline{X}Y+XYZ$

3. Simplify using K-Map   3+3+4=10

   i) $F(X,Y,Z)=(2,3,4,5)$
   ii) $W=\overline{X}\,\overline{Y}Z+\overline{X}YZ+XYZ+X\overline{Y}Z+\overline{X}Y\overline{Z}$
   iii) $F(A,B,C,D)=(0,2,4,5,6,7,8,10,13,15)$

4. Find the answer for the following   2x5 =10

   i)   0.1001-1.011
   ii) 100111/100
   iii) 11110x0.111
   iv) Binary equivalent of $(FA5.E)_{16}$
   v)   Decimal equivalent of $(68.77)_8$

5. What is Flip Flop. Explain JK, D and T Flip Flop with truth table and   3+3+2+2=10
   diagram.

6. Explain four different types shift registers. Design a negative edge   4+3+3 =10
   triggered 2-bit ripple down counter. Give its logic diagram.

7. Describe full subtractor with truth table and logic diagram. Draw the   6+4=10
   logic diagram of full adder using two half adder and gates.

8. Define de-multiplexer. Write the function table for 8:1 multiplexer with   2+4+4 =10
   3data select lines and draw the logic circuit diagram.

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