# BACHELOR OF COMPUTER APPLICATION
## Second Semester
## DIGITAL LOGIC & DESIGN
## (BCA - 06)

**Duration: 3Hrs.** **Full Marks: 70**

**PART A (Objective) =20**
**PART-B (Descriptive)=50**

**PART-B (Descriptive)**

**Duration: 2 hrs. 40 mins.** **Marks: 50**

**1. Answer the following questions (any *five*):** 2×5=10

a) Covert $(378.98)_{10}$ to Octal.

b) Obtain 1's and 2's compliment of the following:

iii) 1010101

iv)0111000

c) State and prove Distributive and Idempotence laws of Boolean algebra.

d) Construct the truth table for AND and OR gate.

e) Explain DeMorgans law.

f) What do you mean by Don't Care Condition?

g) What is Sequential Circuit Explain?

**2. Answer the following questions (any *five*):** 3×5=15

a) What do you mean by shift registers? Explain.

b) Briefly explain binary ripple counter.

c) Write a short note on ASCII and EBCDIC codes.

d) What do you mean by Number System? Write about any 2 number systems.

e) Explain logic gates for XOR, NAND and NOR gates with the help of logic circuit diagram.

f) Explain J-K flip flop with its logic diagram.

g) What are Registers and Counters, explain.

**3. Answer the following questions (any *five*): 5×5=25**

a) Describe the operations performed by the Half-adder and Full-adder arithmetic circuit.

b) Explain the working principle of Decimal Adder.

c) Obtain the truth table for:

$F = xy + xy' + y'z$

$F = xy + x'y' + y'z$

d) Simplify the following function using K-map:

$F = A'B'CD' + A'B'CD + AB'CD' + AB'CD + A'BCD + A'BC'D$

e) Briefly explain decoders with the help of a diagram.

f) Explain design of a simple computer with block diagram.

g) Briefly explain clocked R-S flip flop with the help of logic diagram.

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**Duration: 20 minutes** **Marks – 20**

**PART-A (Objective)**

**Time: 20 mins** **Total Marks: 20**

**I. Choose the correct option:** **1×20=20**

1. How many states do a binary variable has?
   a) 2 b) 3 c) 4
2. The NAND function is complement of which function:
   a) OR b) XOR c) AND
3. A computer system is sometimes divided into 2 functional entities, they are:
   a) Hardware & Software
   b) OS & Software
   c) CPU & OS
4. A function of 'n' variables will have how many minterms:
   a) $2^n$ b) 2n c) 2
5. A combinational circuit that performs the arithmetic addition of 2 bits is called:
   a) Half adder b) Full adder c) JK Flip Flop
6. The input variables of a half adder is called:
   a) Augend & addend b) Sum & carry c) Bits
7. Base of decimal number system is:
   a) 2 b) 8 c) 10
8. Binary equivalent of $(C6)_{16}$ is:
   a) 11000110 b) 11110000 c) 00010011
9. An illustration that is used to visualise the relationships among the variables of a Boolean expression is:
   a) Venn Diagram b) Logic circuit c) K-map
10. Symbol 'Σ' stands for:
    a) ORing of terms b) ANDing of terms c) XORing of terms
11. Each square in K-map represents:
    a) One minterm b) One maxterm c) One variable
12. A four variable K-map will have:
    a) 2 minterms b) 16 minterms c) 8 minterms
13. A decoder converts binary information from 'n' input lines into how many unique output lines:
    a) 2 b) $2^n$ c) $2^2$
14. A flip flop has 2 useful states:
    a) Input & output b) Set & clear c) A & B
15. A flip flop sensitive to pulse duration is called:
    a) Latch b) Register c) Master Slave
16. A register capable of shifting its binary information either to left or right is called:
    a) Shift register b) Register c) Flip flop
17. x(y+z) = xy + xz is an example of:
    a) Demorgans law b) Involution law c) Distributive law
18. (x+y)' = x'y' is an example of:
    a) Commutative law b) Demorgans law c) Absorption law
19. The 'inverter logic gate' has:
    a) 1 input, 1 output b) 2 inputs, 1 output c) 2 input, 2 outputs
20. MSI counters come in 2 categories:
    a) Ripple counters, synchronous counters
    b) Half adder, full adder
    c) JK flip flop, RS flip flop

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