REV-00 MCA/13/18

> MASTER OF COMPUTER APPLICATION First Semester Digital Logic & Design (MCA - 02)

Duration: 3Hrs.

Full Marks: 70

Part-A (Objective) =20 Part-B (Descriptive)=50

(PART-B: Descriptive)

Duration: 2 hrs. 40 mins.

1. Answer the following questions (any five)

- a) Divide $(101101)_2$ by $(110)_2$
- b) Prove that

AB+A(B+C)+B(B+C)=B+AC

- c) What is the octal equivalent of hexadecimal number(B9F.AE)
- d) Simplify the given Boolean expression

 $Y = A + \overline{A} B + \overline{A} \overline{B} C + \overline{A} \overline{B} \overline{C} D$

e) Draw the circuit diagram of full subtractor.

f) Explain the difference between a sequential circuit and combinational circuit.

g) Give the characteristic table and excitation table of SR flip flop.

2. Answer the following questions (any five)

3×5=15

a) Realize an OR gate using a) NAND gate and b) NOR gate

b) Given the logic function of three variables

 $f(A, B, C) = A + \overline{B}C$. Express f in the standard SOP form.

c) Design1X4 demultiplexer.

d) Minimize the following function using K-map.

 $F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$

- e) Design 3X8 decoder using 2X4 decoder.
- f) Construct T flip flop using SR flip flop.

g) Draw the logic diagram of a 4-bit serial in-parallel-out shift register.

2×5=10

Marks: 50

3. Answer the following questions (any five)

a) Convert (1011)₂ and (101)₂ into decimal numbers. Multiply them and then convert the result into binary.

b) Realize following function using 8:1 multiplexer.

 $Y(A,B,C,D) = ABC + ABD + AB\overline{C}\overline{D} + \overline{A}B\overline{C}D$

c) Implement a full adder with two half adders and an OR gate.

d) Design a counter which counts decimal values

0, 1, 3, 4, 5, 6

e) Give the state diagram of J-K flip flop.

f) Design a four bit binary synchronous counter with D flip flop.

g) Write short notes on any one of the following

i) Multiplexer

ii)Shift Register

iii) MOD-6 synchronous counter.

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(MCA - 02)

(The figures in the margin indicate full marks for the questions)

Duration: 20 minutes

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Marks – 20

PART A- Objective Type

Answer all the questions. Each question carries one mark.

Choose correct or the best alternative in the following.

| 1. | Radix of binary number | system is ? |
|----|------------------------|-------------|
| | A) 0 | B) 1 |
| | C) 2 | D) A &B |

| 2. | A group of four bits is known as | |
|----|----------------------------------|--------|
| | A) bit | B)byte |
| | C) nibble | D)word |

- 3. 1's complement representation of decimal number of -17 by using 8 bit representation is

 A) 11101110
 B) 11011101

 C) 11001100
 D) 00010001
- 4. The Gray code for decimal number 6 is equivalent to
 A) 1100
 B) 1001
 C) 0101
 D) 0110
 - 5. The binary equivalent of octal number (367.52) is

 A) 010101111.101010
 B) 011110111.101010

 C) 1111001111.101010
 D) 111110111.101010
- 6. The hexadecimal number 'A0' has the decimal value equivalent to A) 80
 B) 256
 C) 100
 D) 160
- 7. The NAND gate output will be low if the two inputs are
 A) 00
 B) 01
 C) 10
 D) 11
- DeMorgan's first theorem shows the equivalence of A) OR gate and Exclusive OR gate.
 - B) NOR gate and Bubbled AND gate.
 - C) NOR gate and NAND gate.
 - D) NAND gate and NOT gate.

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 $1 \times 20 = 20$

| 9. If X,Y and Z are Boolean variables, A) X+X̄Y C) XYZ | then the expression $X(X+\overline{X}Y) Z(X+Y+Z)$ is equal to B) $X+Y+Z$ D) XZ |
|---|---|
| 10. The simplified form of a logic functionA) ABC) 1 | on Y=AB+ \overline{A} + \overline{B} is B) \overline{A} + \overline{B} D) 0 |
| 11. How many two –input AND and ORA) 2,2C) 3, 3 | gates are required to realize Y=CD+EF+G B)2,3 D) none of these |
| 12. Which of the following is a universalA) ANDC) OR | gate? B) NAND D) NOT |
| 13. A full adder logic circuit will haveA) Two inputs and one outputB) Three inputs and three outputsC) Two inputs and two outputsD) Three inputs and two outputs | |
| 14. The gates required to build a half addeA) Ex-OR gate and NOR gateC) Ex-OR gate and AND gate | er are B) Ex-OR gate and OR gate D) Four NAND gates |
| 15. How many select lines will a 16 to 1 mA) 4C) 5 | nultiplexer will have B) 3 D) 1 |
| 16. One example of combinational circuiA) AdderC) Shift register | t is B) Counter D) Flip-flop |
| 17. A demultiplexer has A) One data input, a number of selection inputs and they have several outputs B) One output and one input C) Several inputs and several outputs. D) Several inputs and one output | |
| 18. How many flip- flops are required for A) 5C) 3 | Mod-16 counter? B) 6 D) 4 |
| 19. In a JK flip-flop, toggle means A) Set Q=1 and Q=0 C) Change the output to the opposite set of the opposite set of | B) Set Q=0 and $\overline{Q} = 1$ state. D) No change in output. |
| 20. A ring counter consisting of five flip- A) 5 statesC) 32 states | flops will have B)10 states D) infinite state. |
