REV-00 BSE/06/12

> B.Sc. ELECTRONICS Third Semester DIGITAL ELECTRONICS (BSE - 301)

Duration: 20 minutes

(PART A - Objective Type)

I. Choose the correct answer:

- 1. Radix of binary number system is ? A) 0 B) 1 C) 2 D) A &B
- 2. A group of four bits is known asA) bit B) byte C) nibble D) word
- 3. 1's complement representation of decimal number of -17 by using 8 bit representation is
 A) 11101110
 B) 11011101
 C) 11001100
 D) 00010001
- 4. The Gray code for decimal number 6 is equivalent to A) 1100 B) 1001 C) 0101 D) 0110
- 5. The binary equivalent of octal number (367.52) is
 A) 010101111.101010
 B) 011110111.101010
 C) 111100111.101010
 D) 111110111.101010
- 6. The hexadecimal number 'A0' has the decimal value equivalent to A) 80 B) 256 C) 100 D) 160
- 7. The NAND gate output will be low if the two inputs are A) 00 B) 01 C) 10 D) 11
- DeMorgan's first theorem shows the equivalence of A) OR gate and Exclusive OR gate.
 - B) NOR gate and Bubbled AND gate.
 - C) NOR gate and NAND gate.
 - D) NAND gate and NOT gate.
- 9. If X,Y and Z are Boolean variables, then the expression $X(X+\overline{X}Y) Z(X+Y+Z)$ is equal to A) $X+\overline{X}Y$ B) X+Y+Z C) XYZ D) XZ
- 10. The simplified form of a logic function $Y=AB+\overline{A}+\overline{B}$ is A) AB B) $\overline{A}+\overline{B}$ C) 1 D) 0
- 11.How many two –input AND and OR gates are required to realize Y=CD+EF+G A) 2, 2 B) 2, 3 C) 3, 3 D) none of these

2016/12

1×20=20

Marks - 20

| 12.Which of the A) AND | following is a univ B) NAND | versal gate? C) OR | D) NOT | |
|--|---|-------------------------------|------------------------------|-----------------------------------|
| 13.A full adder 1 A) Two input C) Two input | ogic circuit will ha and one output and two outputs | ave B) 7 D) 7 | Three inputs Three inputs | and three outputs and two outputs |
| 14.The gates req A) Ex-OR gat C) Ex-OR gat | uired to build a ha te and NOR gate te and AND gate | lf adder are B) E D) F | Ex-OR gate a Four NAND | and OR gate |
| 15.How many se A) 4 | elect lines will a 16 B) 3 C) 5 | to 1 multiple D 1 | exer will hav | e? |
| 16.One example A) Adder C) Shift regist | of combinational B) Counte ter D) Flip-flo | circuit is er op | | |
| 17.One example A) Flip-flop C) Full adder | of sequential circu B) Half ad D) Subtrac | uit is lder ctor | | |
| 18.In a JK flip-fl A) Set Q=1 a B) Set Q=0 a C) Change th D) No change | op, toggle means and $\overline{Q}=0$ and $\overline{Q}=1$ be output to the opple in output. | posite state. | | |
| 19.A ring counte A) 5 states C) 32 states | r consisting of fiv B)10 state D) infinite | re flip-flops w s state | vill have | |
| 20.The binary eq A) 1010 | uivalent of decima B) 0101 | al number (10 C) 0011 |)) is D)1 | 100 |
| | | * * * > | ** | |

-