REV-00 BSE/06/12

### B.Sc. ELECTRONICS Third Semester DIGITAL ELECTRONICS (BSE - 11)

**Duration: 3Hrs.** 

Full Marks: 70

Part-A (Objective) =20 Part-B (Descriptive) =50

#### (PART-B: Descriptive)

Answer any *five* of the following questions:

Duration: 2 hrs. 40 mins.

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Marks: 50

- 1. Answer the following:
  - a) Divide (101101)<sub>2</sub> by (110)<sub>2</sub>.
  - b) Realize an OR gate using a) NAND gate and b) NOR gate.
  - c) Convert the octal number (74213)<sub>8</sub> to hexadecimal equivalent number.
  - d) Simplify the Boolean expression:

 $\overline{A\overline{B} + ABC} + A(B + A\overline{B})$ 

#### 2. Answer the following:

- a) Give the BCD code for the decimal number (874).
- b) Convert (643)<sub>10</sub> into its Excess-3 code.
- c) Convert the Gray code (1011001) to binary number.
- d) Simplify the expression:  $AB + \overline{AC} + A\overline{B}C(AB+C)$
- e) Convert the binary number  $(10101101)_{10}$  to its Gray code.



(2+2+3+3=10)

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 $(2 \times 5 = 10)$ 

#### 3. Answer the following:

a) Prove the following Boolean expression:

# 1. $(A+B)(\overline{A}\overline{C}+C)(\overline{B}+A\overline{C})=\overline{A}B$

- 2.  $\overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$
- b) Describe the NOR gate. Specify its symbol and write its truth table.

### 4. Answer the following:

- a) Convert the hexadecimal number (2AF.31)<sub>16</sub> to its decimal equivalent.
- b) Represent -44 in 2's complement form using 8-bits.
- c) Represent -77.25 in 8 bit 1's complement form.
- d) What is De Morgan's theorem?

### 5. Answer the following:

- a) What is encoder?
- b) Write short notes on the following: (any two)
  - 1. Timer IC 555

2. R-2R ladder network.

3. Shift Registers.

### 6. Answer the following:

- a) Design a full adder using half adders and OR gate.
- b) Minimize the following function using K-map.

1. 
$$F(A,B,C,D) = A\overline{B}C\overline{D} + \overline{A}\overline{B}CD + ACD + A\overline{B}D + AD + \overline{A}B\overline{C}$$

2.  $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$ 

### 7. Answer the following:

- a) Design a full subtractor from the truth table.
- b) Design a 1x4 demultiplexer.
- c) Explain the principle of operation of S-R flip-flop.

(3+3+4=10)

#### (3+3+4=10)

# (3+2+3+2=10) uivalent.

(2+4+4=10)

## 8. Answer the following:

- a) Give the characteristic table, excitation table and the state diagram of J-K flip-flop.
- b) Design a 4x16 decoder using 2x4 decoders.
- c) Design a 4x1 MUX.

a)

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## (5+3+2=10)

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# B.Sc. ELECTRONICS Third Semester DIGITAL ELECTRONICS (BSE - 11)

# **Duration: 20 minutes**

# (PART A- Objective Type)

# I. Choose the correct answer:

- 1. Radix of binary number system is \_\_?A) 0B) 1C) 2D) A &B
- 2. A group of four bits is known as<br/>A) bitB) byteC) nibbleD) word
- 3. 1's complement representation of decimal number of -17 by using 8 bit representation is
  A) 11101110
  B) 11011101
  D) 00010001
- 4. The Gray code for decimal number 6 is equivalent to A) 1100 B) 1001 C) 0101 D) 0110
- 5. The binary equivalent of octal number (367.52) isA) 010101111.101010C) 111100111.101010D) 111110111.101010
- 6. The hexadecimal number 'A0' has the decimal value equivalent to A) 80 B) 256 C) 100 D) 160
- 7. The NAND gate output will be low if the two inputs are A) 00 B) 01 C) 10 D) 11

8. De Morgan's first theorem shows the equivalence of
A) OR gate and Exclusive OR gate
C) NOR gate and NAND gate
B) NOR gate and Bubbled AND gate
D) NAND gate and NOT gate

- 9. If X,Y and Z are Boolean variables, then the expression  $X(X+\overline{X}Y) Z(X+Y+Z)$  is equal to A)  $X+\overline{X}Y$  B) X+Y+Z C) XYZ D) XZ
- 10. The simplified form of a logic function $Y=AB+\overline{A}+\overline{B}$  isA) ABB)  $\overline{A}+\overline{B}$ C) 1D) 0
- 11.How many two –input AND and OR gates are required to realize Y=CD+EF+G?A) 2,2B) 2,3C) 3,3D) none of these
- 12. Which of the following is a universal gate?A) ANDB) NANDC) ORD) NOT

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1×20=20

Marks - 20

<ul><li>13.A full adder logic circuit will have</li><li>A) Two inputs and one output</li><li>C) Two inputs and two outputs</li></ul>			<ul><li>B) Three inputs and three outputs</li><li>D) Three inputs and two outputs</li></ul>		
	14.The gates require A) Ex-OR gate a C) Ex-OR gate a	te B) Ex-OR gate and OR gate te D) Four NAND gates		ate and OR gate ND gates	
	15.How many select A) 4 B	t lines will 5) 3	a 16 to 1 mu C) 5	ltiplexer will	D) 1
	16.One example of A) Adder C) Shift register	combinatio	nal circuit is B) Counter D) Flip-flop		
	17.One example of s A) Flip-flop C) Full adder	sequential o	circuit is B) Half addo D) Subtracto	er Dr	
	18. In a JK flip-flop, toggle meansA) Set Q=1 and $\overline{Q}=0$ B) Set Q=0 and $\overline{Q}=1$ C) Change the output to the opposite stateD) No change in output				
	19.A ring counter co A) 5 states C) 32 states	onsisting o	f five flip-flo B) 10 states D) infinite s	ops will have tate	
•	20.The binary equiv A) 1010 B	valent of dec $()$ 0101	cimal numbe C) 00	er (10) is 11	D) 0010

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