MASTER OF COMPUTER APPLICATION

Second Semester

Computer Organization and Architecture

(MCA-07)

Duration: 3Hrs. **Full Marks: 70**

(PART-B: Descriptive)

Duration: 2 hrs. 40 mins. **Marks: 50**

1. Answer any five questions **5×2=10**

(a) What do you mean by computer organization and computer architecture?

(b) What is interrupt?

(c) Write down the overflow rule.

(d) Write the types of operands.

(e) What is hit ratio?

(f) What are user visible registers?

(g) What are micro operations? Explain the Fetch cycle.

2. Answer any five questions **5×3=15**

(a) Explain multiple bus hierarchies.

(b) What are serial interfaces and parallel interfaces?

(c) Write about instruction cycle with interrupt.

(d) Explain the various mapping techniques.

(e) Explain page replacement and segmentation.

(f) Explain the Interrupt cycle.

(g) Explain the execute cycle.

PTO...

3. Answer any five questions **5×5=25**

(a) Write down the steps for interrupt processing.

(b) What is meant by DMA? Write about DMA transfer.

(c) Draw and describe I/O module structure.

(d) Briefly explain the computer memory system with diagram.

(e) Explain the various addressing modes. Give the difference between the RISC and CISC instruction.

(f) Describe the operations that are performed by control and status registers.

(g) Draw the block diagram of a control unit and explain its different inputs/outputs.

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REV-00
MCA /17/22 2013/02

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(The figures in the margin indicate full marks for the questions)

Duration: 20 minutes **Marks – 20**

(PART A- Objective)

Choose (✓) the correct response(s) in each of the multiple choice questions:

1. The ability to temporarily halt the CPU and use this time to send information on buses is called
   (A) Direct memory access
   (B) Vectoring the interrupt
   (C) System interrupts
   (D) Cycle stealing

2. What is the control unit's function in the CPU?
   (A)To transfer data to primary storage
   (B) To store program instruction
   (C) To perform logic operations
   (D) To decode program instruction

3. Interrupts which are initiated by an instruction are
   (A) Internal (B) External
   (C)Hardware (D) Software

4. CPU does not perform the operation
   (A) data transfer (B) logic operation
   (C) arithmetic operation (D)all of above

5. In a DMA write operation the data is transferred
   (A) from I/O to memory.
   (B) from memory to I/O.
   (C) from memory to memory.
   (D) from I/O to I/O.

6. Which of the following is true with respect to EEPROM?
   (A) contents can be erased byte wise only.
   (B) contents of full memory can be erased together.
   (C) contents can be erased using ultra violet rays
   (D) contents can not be erased

7. The PCI bus is the important bus found in all the new Pentium systems because
   (A) It has plug and play characteristics
   (B) It has ability to function with a 64 bit data bus
   (C) Any Microprocessor can be interfaced to it with PCI controller or bridge
   (D) All of the above

8. Which of the following statement is true?
   (A) The group of machine cycle is called a state.
   (B) A machine cycle consists of one or more instruction cycle.
   (C) An instruction cycle is made up of machine cycles and a machine cycle is made up of number of states.
   (D) None of the above

9. The most relevant addressing mode to write position independent code
   (A) Direct mode
   (B) Indirect mode
   (C) Relative mode
   (D) Indexed mode

10. Where does a computer add and compare data?
   (A) Hard disk
   (B) Floppy disk
   (C) CPU chip
   (D) Memory chip

11. In which addressing mode the operand is given explicitly in the instruction itself?
   (A)Absolute mode
   (B)Immediate mode
   (C) Indirect mode
   (D) Index mode

12. The addressing mode used in the instruction PUSH B is
   (A) Direct
   (B)Register
   (C) Register indirect
   (D) Immediate

13. Which of the following need not necessarily be saved on a context switch between processes?
   (A)General purpose register
   (B)Translation lookaside buffer
   (C) Program counter
   (D) All of these

14. Processors of all computers, whether micro, mini or mainframe must have
   (A) ALU
   (B) Primary Storage
   (C) Control unit
   (D) All of above

15. A time sharing system imply
(A)more than one processor in the system
(B)more than one program in memory
(C) more than one memory in the system
(D) None of above

16. A CPU generally handles an interrupt by executing an interrupt service routine
(A) as soon as an interrupt is raised
(B) by checking the interrupt register at the end of fetch cycle
(C) by checking the interrupt register after finishing the executing the current instruction
(D) by checking the interrupt register at fixed time intervals

17. The register that holds the base of the segment
(A) Segment pointer
(B) Index register
(C) Stack pointer
(D) Condition codes

18. The Register that contains the next instruction to be fetched is
(A) Program Counter
(B) Instruction register (IR)
(C) Memory Address register
(D) Memory Buffer Register

19. External Data paths
(A) Move data between registers
(B) Move data between registers and ALU
(C) Links registers to memory and I/O modules
(D) None of the above

20. The control unit causes the processor to step through a series of micro operations known as
(A) Execution
(B) Sequencing
(C) Opcode
(D) Operand

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