REV-00
BCA/ 08 /18 2013/02

BACHELOR OF COMPUTER APPLICATION

Second Semester

Digital Logic Design

(BCA - 06)

Duration: 3Hrs. **Full Marks: 70**

(PART-B: Descriptive)

Duration: 2 hrs. 40 mins. **Marks: 50**

I. Answer the following questions (any five) **2 x 5=10**

1. Explain the following terms:
   a) bit b)byte c)nibble d)word length
2. What do you mean by self complementing code? Write two self complementing codes.
3. What do you mean by error-correcting codes? Define checksums.
4. Draw the logic symbols and construct the truth tables of the following gates:
   a) AND b) OR c) NAND d) NOR
5. State and prove De-Morgan's Theorem.
6. Reduce the expression A`B`+A`B+AB using mapping.
7. What is a Flip flop? Explain.

II. Answer the following questions (any five) **3 x 5=15**

1. Represent the following decimal numbers in 8-bit
   a)Sign magnitude form
   b)1's complement form
   c)2's complement form
2. Convert the Gray code 1101 to binary.
3. Show that AB+ (A+B) ` is equivalent to A (x-nor) B.
4. Prove the idempotence laws
   a)A.A=A
   b)A+A=A
5. Implement a half adder using NAND Logic.
6. How does a J-K Flip flop differ from an S-R Flip flop in its basic operation.
7. What is a D-Flip flop? Explain.

III. Answer the following questions (any five) **5 x 5=25**

1. Multiply the following using computer method – 1111x100.
2. Show that A(x-or) B=AB`+A`B and construct the corresponding logic diagram.
3. Reduce the following expression ∏ M (2, 8, 9, 10, 11, 12, 14) and implement it in universal logic.
4. Construct the truth table and draw the logic diagram of a Full Adder.
5. Construct the truth table and draw the logic diagram of a Half subtractor
6. What is a Decoder. Draw the logic diagram and construct the truth table for 3-line to 8-line Decoder.
7. What is a Multiplexer? Draw the logic diagram and construct the truth table for a 4-input Multiplexer.

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(The figures in the margin indicate full marks for the questions)

Duration: 20 minutes **Marks – 20**

PART A- Objective Type

I. Choose the correct option for the following questios: **1×20=20**

1. The NAND gate output will be low if the two inputs are

(A) 00 (B) 01 (C) 10 (D) 11

2. What is the binary equivalent of the decimal number 368

(A) 101110000 (B) 110110000 (C) 111010000 (D) 111100000

3. The decimal equivalent of hex number 1A53 is

(A) 6793 (B) 6739 (C) 6973 (D) 6379

4. The number of control lines for a 8 – to – 1 multiplexer is

(A) 2 (B) 3 (C) 4 (D) 5

5. The Gray code for decimal number 6 is equivalent to

(A) 1100 (B) 1001 (C) 0101 (D) 0110

6. The 2's complement of the number 1101101 is

(A) 0101110 (B) 0111110 (C) 0110010 (D) 0010011

7. The gates required to build a half adder are

(A) EX-OR gate and NOR gate (B) EX-OR gate and OR gate

(C) EX-OR gate and AND gate (D) Four NAND gates.

8. The code where all successive numbers differ from their preceding number by single bit is

(A) Binary code. (B) BCD. (C) Excess – 3. (D) Gray.

9. In a JK Flip-Flop, toggle means

(A) Set Q = 1 and Q = 0.

(B) Set Q = 0 and Q = 1.

(C) Change the output to the opposite state.

(D) No change in output.

10. How many AND gates are required to realize Y = CD+EF+G
(A) 4 (B) 5 (C) 3 (D) 2

11. For JK flip flop with J=1, K=0, the output after clock pulse will be
(A) 0. (B) 1 (C) high impedance. (D) no change.

12. The result of adding hexadecimal number A6 to 3A is
(A) DD. (B) E0. (C) F0. (D) EF.

13. A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate?
(A) OR (B) AND (C) XOR (D) NAND

14. Karnaugh map is used for the purpose of
(A) Reducing the electronic circuits used.
(B) To map the given Boolean logic function.
(C) To minimize the terms in a Boolean expression.
(D) To maximize the terms of a given a Boolean expression.

15. A full adder logic circuit will have
(A) Two inputs and one output.
(B) Three inputs and three outputs.
(C) Two inputs and two outputs.
(D) Three inputs and two outputs.

16. The hexadecimal number 'A0' has the decimal value equivalent to
(A) 80 (B) 256 (C) 100 (D) 160

17. When simplified with Boolean Algebra (x + y) (x + z) simplifies to
(A) x (B) x + x(y + z) (C) x(1 + yz) (D) x + yz

18. -8 is equal to signed binary number
(A) 10001000 (B) 00001000 (C) 10000000 (D) 11000000

19. The chief reason why digital computers use complemented subtraction is that it
(A) Simplifies the circuitry.
(B) Is a very simple process.
(C) Can handle negative numbers easily.
(D) Avoids direct subtraction.

20. In a positive logic system, logic state 1 corresponds to
(A) positive voltage (B) higher voltage level (C) zero voltage level (D) lower voltage level

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