7. a. Define the term Fan- in and Fan- out for logic circuit. 2+8 =10

b. With the help of neat diagram, explain the working of two input TTL NAND logic.

8. a. Design a Synchronous 3-bit down counter. 6+4 =10

b. Explain the operation of a serial in, parallel out shift register.

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M. Sc. ELECTRONICS
SECOND SEMESTER
DIGITAL ELECTRONICS SYSTEM & DESIGN
MSE-201
(Use Separate Answer Scripts for Objective & Descriptive)

Duration : 3 hrs. **Full Marks : 70**

(PART-A : Objective)

Time : 20 min. **Marks : 20**

Choose the correct answer from the following: ***1×20=20***

1. A group of 8 bits is known as
   a. A nibble
   b. A byte
   c. A bit
   d. An octal number

2. 1's complement of 1's complement of the binary number 10110011
   a. 01001100
   b. 10110011
   c. 01001101
   d. 10111010

3. ASCII code is a ____ bit code.
   a. 6
   b. 7
   c. 8
   d. 10

4. A bubbled OR gate is equivalent to a
   a. AND gate
   b. NAND gate
   c. NOR gate
   d. X-OR gate

5. The output of a NAND gate is low
   a. Only when all inputs are low
   b. Only when all inputs are high
   c. Only when atleast one input is high
   d. All of the above

6. An all or nothing gate is the other name of
   a. AND gate
   b. OR gate
   c. NAND gate
   d. NOR gate

7. For checking the parity of a digital word, it is preferable to use
   a. AND gate
   b. NAND gate
   c. XOR gate
   d. XNOR gate

8. An n variable K-Map can have
   a. n^2 cells
   b. 2^n cells
   c. n^n cells
   d. n^{2n} cells

9. The total number of 1's present in a term is called
   a. index
   b. weight
   c. logic levels
   d. term number

10. The number of cells in a 6 variable K-Map is
    a. 6 b. 12
    c. 36 d. 64

11. Each term in the standard POS form is called
    a. minterm b. maxterm
    c. Don't care d. literal

12. The number of flipflops required for a mod 12 ring counter
    a. 4 b. 6
    c. 12 d. 24

13. A mod-2 counter followed by mod-5 counter is same as
    a. mod-5 counter followed by mod-2 counter b. Mod-10 counter
    c. Mod-7 counter d. None of the above

14. The fastest logic family is
    a. TTL b. ECL
    c. IIL d. MOS

15. The fastest ADC is
    a. Counter type ADC b. Flash type ADC
    c. Successive approximation ADC d. Dual slope ADC

16. The logic family which consumes maximum power is
    a. ECL b. TTL
    c. CMOS d. MOS

17. The toggle mode for JK- flipflop is
    a. J=0, K=0 b. J=0, K=1
    c. J=1, K=0 d. J=1, K=1

18. For a flipflop with provisions of preset(PRE) and clear(CLR)
    a. PRE and CLR are performed simultaneously b. While presetting, clear is disabled
    c. While clearing, preset is disabled d. Both b and c

19. Master slave configuration is used in flipflop to
    a. Increase its clocking rate b. Reduce power dissipation
    c. Eliminate race around condition d. None of the above

20. A multiplexer is also known as
    a. A data accumulator b. A data restorer
    c. A data selector d. A data distributer

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(PART-B : Descriptive)

Time : 2 hrs. 40 min. **Marks : 50**

[Answer question no.1 & any four (4) from the rest]

1. a. Design a 4 bit Weighted Resistor DAC. 6+4 =10
   b. Why is the tracking type ADC faster than the counter type ADC?

2. a. Distinguish between SRAMs and DRAMs. 5+2+3 =10
   b. What is random access memory?
   c. What does a 32*8 ROM contain?

3. a. With the help of a logic diagram and truth table, explain an octal to binary encoder. 5+5 =10
   b. Realize a full adder.

4. a. Obtain the minimal expression using tabular method $\sum m(1,2,3,5,6,7,8,9,12,13,15)$ 6+4 =10
   b. Reduce the expression $f=\Pi(1,5,6,7,11,12,13,15)$

5. a. What is an XS-3 code? What are the invalid states in XS-3 code? 4+2+4 =10
   b. Why is ASCII code a 7 bit code?
   c. How do you convert a Gray number to binary? Explain with example

6. a. Add the binary number 10111.101+ 110111.01 2×5 =10
   b. Subtract 1100.10 - 111.01
   c. Represent -17 in 1's complement form.
   d. Subtract the hexadecimal numbers BC5- A2F
   e. Subtract the octal numbers 462-175