REV-01
BCA/07/15

2025/12

SET A

BACHELOR OF COMPUTER APPLICATION
FIRST SEMESTER (REPEAT)
DIGITAL LOGIC & DESIGN
BCA-102

[USE OMR FOR OBJECTIVE PART]

Duration: 3 hrs. **Full Marks: 70**

Objective

Time: 30 min. **Marks: 20**

Choose the correct answer from the following: *1X20=20*

1. Which number system has a base 8?
   a. Hexadecimal
   b. Octal
   c. Binary
   d. Decimal

2. DeMorgan's Law states that
   a. (A+B)' = A'*B
   b. (AB)' = A' + B'
   c. (AB)' = A' +B
   d. (AB)' = A + B

3. The binary subtraction of 0 – 1 =?
   a. Difference = 0, borrow = 0
   b. Difference = 1, borrow = 0
   c. Difference = 1, borrow = 1
   d. Difference = 0, borrow = 1

4. (A + B)(A' * B') = ?
   a. 1
   b. 0
   c. AB
   d. AB'

5. How many AND gates are required to realize Y = CD + EF + G?
   a. 4
   b. 5
   c. 3
   d. 2

6. Which device has one input and many outputs?
   a. De multiplexer
   b. Multiplexer
   c. Counter
   d. Flip-flop

7. The D flip-flop has ___ inputs
   a. 1
   b. 3
   c. 2
   d. 4

8. What is the addition of the binary numbers 11011011010 and 010100101?
   a. 0111001000
   b. 1100110110
   c. 1110111111
   d. None of the above

9. 2's complement of binary number 0101 is
   a. 1011
   b. 1110
   c. 1010
   d. 1101

10. How many select lines would be required for an 8-line-to-1-line multiplexer?
    a. 2 b. 4
    c. 8 d. 3

11. The Universal gate is _____
    a. NAND gate b. OR gate
    c. AND gate d. None of the above

12. The basic storage element in a digital system is _____
    a. Counter b. Flip-flop
    c. Multiplexer d. Encoder

13. A decoder converts N inputs to _____ outputs
    a. N b. N^2
    c. 2^N d. N^N

14. Applying the distributive law to the expression A(B+C'+D), we get
    a. AB+AC+AD b. ABCD
    c. A+B+C+D d. AB+AC'+AD

15. The binary number 10011 is equivalent to the decimal number _____
    a. 12 b. 21
    c. 19 d. None of these

16. The number of inputs in a half adder is?
    a. 8 b. 11
    c. 2 d. 32

17. The Boolean expression Y = A+B is logically equivalent to what single gate?
    a. NAND b. AND
    c. NOR d. OR

18. What is the binary subtraction of 101001 - 010110 =?
    a. 010011 b. 011001
    c. 100110 d. 010010

19. In the toggle mode, a JK flip-flop has
    a. J = 0, K = 1 b. J = 1, K = 1
    c. J = 0, K = 0 d. J = 1, K = 0

20. How much input and output needed for demultiplexer?
    a. Many outputs to one input b. One input many outputs
    c. One input one output d. None of these

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Descriptive

Time : 2 hrs. 30 min. Marks : 50

[Answer question no.1 & any four (4) from the rest]

1. a. Write the truth table and draw logic circuit diagram for Half adder. 5+5=10
   b. Explain 1 X 4 Demultiplexer.

2. a. Perform the following subtractions using 1's and 2's complement methods: $1101_{(2)} - 1010_{(2)}$ 4+3+3=10
   b. Find the result $110011_{(2)} + 101100_{(2)}$
   c. Convert $AB5_{(16)}$ to Binary.

3. How many types of shift registers are available? Explain each of them with diagram. 10

4. Write truth table and logic diagram for AND, OR, NAND, NOR and Ex OR. 10

5. Minimize the following with the help of K-map and draw the logic circuit for the minimized expression. 5+5=10
   I. $F=\Sigma(2,3,4,5,6,7,9,12,13,14,15)$
   II. $F=\Sigma(0,1,3,4,5,7,12,13,15)$

6. a. How we create a Master- Slave flip flop using two JK flip flop? 4+6=10
   b. Explain mod-10 negative edge asynchronous up counter with diagram.

7. **Simplify the following expression** 5+5=10
   I. $X=AB+A(B+C)+B(B+C)$
   II. $X=AB+A'B'C+A$

8. **Write short notes on any two:** 5+5=10
   I. SR Flip Flop
   II. ASCII Code
   III. 8 x 1 Multiplexer

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