**MASTER OF COMPUTER APPLICATION**
**SECOND SEMESTER**
**COMPUTER ORGANIZATION**
**MCA – 202**
**( Use Separate Answer Scripts for Objective & Descriptive )**

**Duration : 3 hrs.** **Full Marks : 70**

**( PART-A : Objective )**

**Time : 20 min.** **Marks : 20**

***Choose the correct answer from the following:*** ***1×20=20***

1. FPGA means
   a. Field Programmable Gate Array
   b. Forward Programmable Gate Array
   c. Forward Parallel Gate Array
   d. Field Parallel Gate Array

2. What is mean by ALU
   a. Arithmetic logic upgrade
   b. Arithmetic logic unit
   c. Arithmetic local unsigned
   d. Arithmetic logic unsigned

3. Which one of the following is not a vectored interrupt?
   a. TRAP.
   b. INTR
   c. RST 3.
   d. RST 7.5.

4. HLT opcode means
   a. load data to accumulator.
   b. store result in memory.
   c. load accumulator with contents of register.
   d. end of program.

5. Type of ROM which is manufactured without having any initial storage in it is termed as
   a. PROM
   b. EROM
   c. BROM
   d. DROM

6. Access store from which data can be read and can be written on it is classified as
   a. read only memory
   b. random access memory
   c. random only memory
   d. read access memory

7. Switching from one process to another. This swapping is called a
   a. Process switch
   b. Context switch
   c. Exchange
   d. both a and b

8. Flash memories have limited number of block's write cycles, these cycles must be at least
   a. 1000
   b. 10,000
   c. 100,000
   d. 100,000,00

9. In 32-bit addressing mode, address field is either 1 byte or
   **a.** 2 bytes **b.** 3 bytes **c.** 4 bytes **d.** 5 bytes

10. If a comparing instruction and branch instruction uses some architectures, to treat these comparisons chooses as
   **a.** Error **b.** Exceptions
   **c.** Special cases **d.** All of the above

11. Addressing mode which is set to index arrays, is applied to indexed addressing mode, in computers is
   **a.** Scaled addressing mode **b.** Register indirect addressing mode
   **c.** Register addressing mode **d.** Immediate addressing mode

12. Simplest scheme to handle branches is to
   **a.** Flush pipeline **b.** Freezing pipeline
   **c.** Depth of pipeline **d.** Both a and b

13. The DMA transfers are performed by a control circuit called as
   **a.** Device interface **b.** DMA controller
   **c.** Data controller **d.** Overlooker

14. DMA stands for
   **a.** Direct Memory Access **b.** Double Memory Access
   **c.** Duplicate Memory Access **d.** None of the Above

15. Which is not an type of Interrupts
   **a.** Vectored **b.** Non-Vectored
   **c.** Priority **d.** Accessible

16. After the completion of the DMA transfer the processor is notified by
   **a.** Acknowledge signal **b.** Interrupt signal
   **c.** WMFC signal **d.** None of the above

17. The DMA controller has _____ registers
   **a.** 1 b. 2 c. 3 d. 4

18. The controller is connected to the ____
   **a.** Processor BUS **b.** System BUS
   **c.** External BUS **d.** None of the above

19. The technique where the controller is given complete access to main memory is
   **a.** Cycle stealing **b.** Memory stealing
   **c.** Memory Con **d.** Burst mode

20. The registers of the controller are _____
   **a.** 64 bits **b.** 34 bits
   **c.** 32 bits **d.** 16 bits

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Contd...

## ( PART-B : Descriptive )

**Time : 2 hrs. 40 min.** **Marks : 50**

*[ Answer question no.1 & any four (4) from the rest ]*

1. What is Interrupt ? Define Interrupt 10

2. a. What is Direct Memory Access? 5+5=10
   b. Expalin the working principle of DMA with neat diagram.

3. a. What is Computer Memory 4+6 =10
   b. Explain different types of Computer Memory.

4. Give the pin-out diagram of 8085 microprocessor with pin details. 10

5. a. What is Instruction format? 5+5=10
   b. Expalin one address instruction with the following example :
   X=(A+B) * (C+D) * E

6. Write a assembly language program to find 1's compliment of a 16 bit number. Write the significance of the steps. 6+4 =10

7. a. What is Asynchronous Data Transfer? 4+6=10
   b. Explain Source Initiated Handshaking Mechanism.

8. Define RISC & CISC? What is Stack Organization? Explain with a suitable example. 3+3+4 =10

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